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Design Considerations for Class-D Audio Power Amplifiers

Application Report

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Design Considerations for Class-D Audio Power Amplifiers

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ABSTRACT

This application report provides background information, general equations, and component selection criteria for proper design and implementation of the Texas Instruments class-D audio power amplifiers. Topics include class-D switching and charge pump circuits, signal conditioning of the audio inputs and outputs for both the class-D and class-AB headphone amplifiers, IC control and indicator circuits, power supply decoupling, and PCB layout.

1 Introduction

Circuit design and layout plays a large role in creating or reducing distortion in class-D audio power amplifiers. The high-frequency-switching characteristics of class-D output stages offer some interesting design challenges over conventional class-AB amplifiers. This application report provides the background information necessary to properly design Texas Instruments (TI™) class-D stereo audio power amplifiers into an audio solution.

Texas Instruments offers several class-D stereo audio power amplifiers, each of which is featured on an evaluation module (EVM), available from TI. All information appearing in this report originated from the design of the SLOP204 EVM, which features the TPA005D14 class-D stereo audio power amplifier IC. The TPA005D14 EVM is capable of driving 2 W into a 4-Ω load from a 5-V power supply. This and similar TI EVMs allow customers to evaluate the performance of TI's class-D audio products without spending the time and resources normally required to design and build a test circuit. In addition, each EVM is compatible with the TI plug-n-play audio amplifier evaluation platform, which provides the power, standard audio interconnects, signal conditioning, and speakers required to operate the audio system.

TI class-D EVMs are available with or without an internal class-AB headphone amplifier circuit. The ICs with the headphone circuit are equipped with the necessary internal interface logic to select between the class-D and headphone modes of operation. Each EVM includes onboard pushbutton switches for manual muting and shutdown, and input pins for logic control of mode, mute, and shutdown. A miniature stereo headphone jack is mounted on the EVMs that have the internal headphone amplifier to allow convenient connection of headphones.

The modules have single in-line header connector pins mounted to the underside of the boards. These pins allow the module to be plugged into the plug-n-play platform, which automatically makes all of the signal input and output, power, and control connections to the module. The module connection pins are on 0.1-inch centers to allow easy use with standard perf board- and plug board-based prototyping systems, or for direct wiring into existing circuits and equipment when used stand-alone.

These EVMs and the plug-n-play platform can be found at the TI web site: http://www.ti.com/sc/apa.

2   Class-D Amplifier Circuits

The class-D amplifier IC consists of an analog input circuit section, switching circuit, a pulse-width modulation circuit, charge pump and gate drive circuit, and an output circuit. All of these circuits, except the pulse-width modulator, require external components for operation. This section focuses on the criteria for determining these external components.

2.1   Input Circuit

The input stage of each channel of the class-D amplifier is a differential amplifier, which means filters are required for both the noninverting and the inverting inputs as shown in Figure 1. These input filters serve two purposes: they set the low frequency corner, f_{LO}, and they block dc voltages and currents.
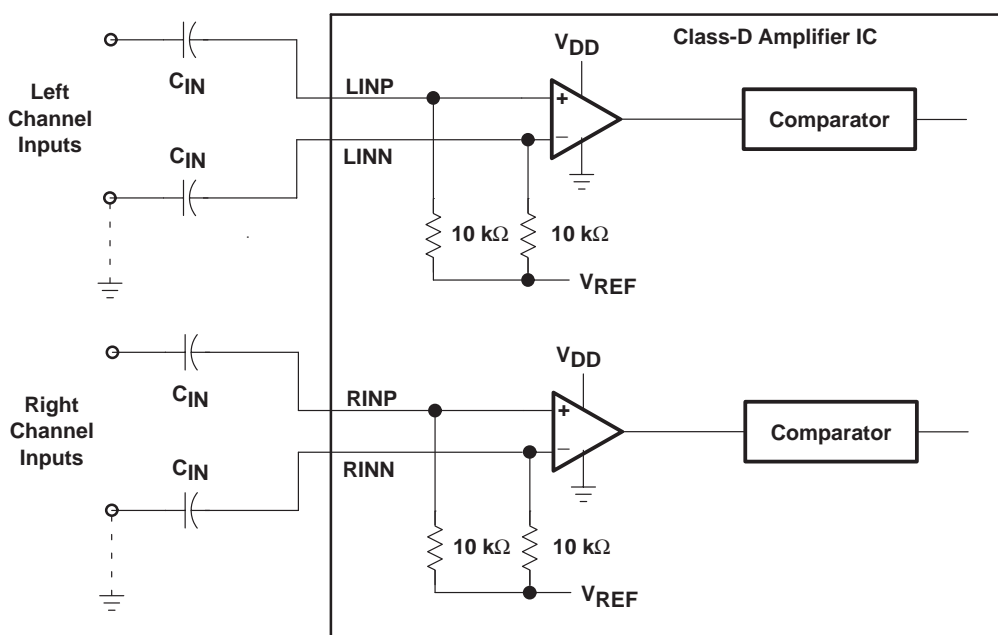

Figure 1. Class-D Input Circuit and Filter

Each filter consists of one external capacitor (C_{IN}) in series with the internal resistance (R_{IN}) of the amplifier input. Such a configuration creates a first-order, high-pass filter (HPF) with a –3 dB cutoff frequency of

$$f_{LO} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \qquad (1)$$

where R = R_{IN} = 10 kΩ ±20% (typical) and C = C_{IN} = 1 µF for a –3 dB value of 15.9 Hz for the class-D EVMs. The f_{LO} can be easily adjusted by changing the value of C_{IN}.

The inputs can also be driven single-ended by applying the audio input signal to the noninverting input and ac-grounding the inverting input as shown by the dashed line in Figure 1. This is necessary to avoid mismatching the impedance of the two inputs, which creates a differential voltage and a potential for popping in the speakers when power is applied to the system. The capacitor also prevents dc current flow from the internal voltage reference to ground.

The internal gain of the class-D amplifier limits the input voltage to a maximum of

$$V_{IN} = \frac{\sqrt{P_O \cdot R_L}}{A_V}$$

(2)

where P_O is the maximum output power, R_L is the dc load resistance, and A_V is the internal gain of the class-D amplifier. The large gain and low input currents of the class-D amplifier reduces the input voltage to much less than 1 V and allows the use of small, ceramic capacitors on the inputs.

The input capacitors should be placed as close to the input pins as possible to reduce noise pickup. Connecting the inputs differentially further reduces the input noise. Surface-mount, ceramic capacitors are readily available in 0805 for X7R and Y5V, and can even be found in 0603 Y5V. Ceramic capacitors are preferred over electrolytic for their small size, low equivalent series resistance (ESR), low noise, and longer life of the component.

2.2 Output Circuit

The class-D amplifier outputs are driven by heavy-duty DMOS transistors in an H-bridge configuration. These transistors are either fully on or off, which reduces the R_{DSON} and the power dissipated in the device, increasing efficiency. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. There are several options available as to what type of filtering should be used to recover the audio signal. The output may be directly applied to the speaker if the speaker is inductive at the class-D switching frequency and EMI is not an issue, or a half filter could be used.[1] However, for this application it is assumed that EMI is a consideration, and the focus is therefore the full output filter shown in Figure 2.
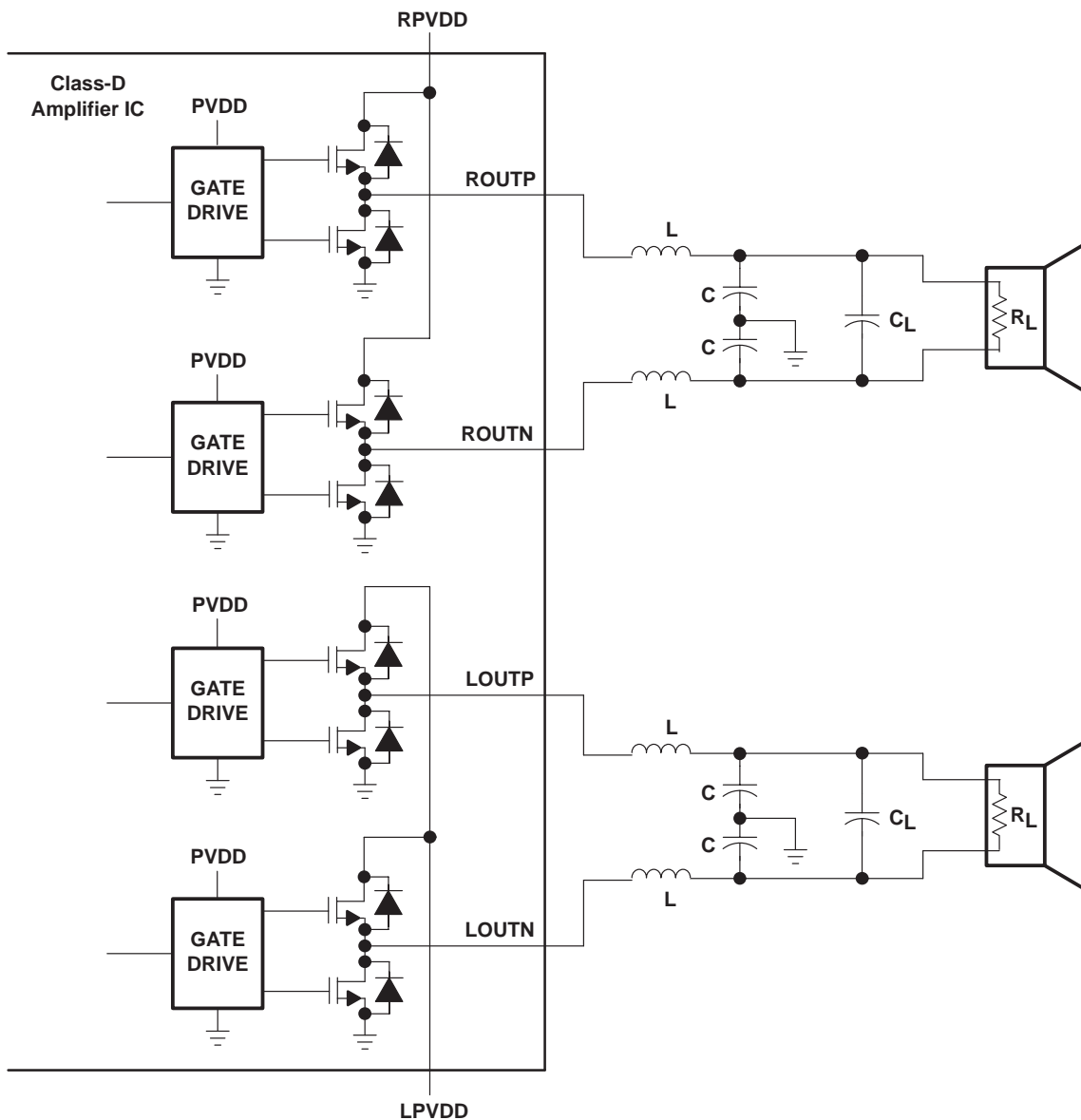

Figure 2. Class-D Output Circuit and Filter

The main goal of the output filter is attenuation of the high frequency switching component of the class-D amplifier while preserving the signals in the audio band. This describes the characteristic of a low-pass filter (LPF), which is specified by its cutoff frequency (–3 dB point), gain and ripple in the pass band, and attenuation in the stop band. The order of the filter determines how many poles exist at the same frequency, with each order increasing the attenuation above the cutoff frequency by –20 dB per decade. The switching frequency (f_S) of the class-D amplifier can influence the choice of the filter order — the higher the f_S, the lower the order required to achieve a given attenuation within a specified passband. This would seem to dictate the use of the highest switching frequency possible. The tradeoff is that increasing f_S increases the switching losses and the EMI, and decreases the efficiency of the amplifier.

A second order LPF reduces f_S by –40 dB per decade to one percent of its prefiltered value. A 5-V signal at 250 kHz is reduced by –40 dB over one decade to 50 mV. If increased attenuation is desired, two alternatives remain; a higher order filter could be implemented, increasing the number of components and the cost, or f_S could be increased, lowering the overall efficiency and increasing EMI.

2.2.1 Filter Design

The output filter is a simple, second-order, LC-type filter designed using a Butterworth approximation. This type of filter is desired for the relatively flat pass-band response it provides and the small number of parts it requires. The transfer function for a second order Butterworth approximation is

$$H(s) \; = \; \frac{1}{s^2 + \sqrt{2} \; s + 1} \tag{3}$$

The first step is to realize the circuit and derive the transfer function, beginning with a half circuit model and moving to the full-bridge circuit. The half circuit model of the BTL output is shown in Figure 3, with half of the desired dc load resistance (R_H) of the speaker shown. The input signal (V_{IN}) is the 250-kHz square wave output of the class-D amplifier, while the output (V_O) is the voltage developed across the speaker.
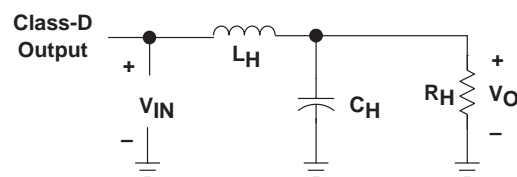

Figure 3. BTL Half-Circuit Model

Converting the inductance and capacitance into S-domain representations ($L \Rightarrow Ls$ and $C \Rightarrow 1/Cs$), solving for the transfer function, and manipulating the terms into the form of equation 3 gives the transfer function for the half-circuit model.

$$H(s) = \frac{V_O(s)}{V_{IN}(s)} = \frac{\frac{1}{L_H \cdot C_H}}{s^2 + \frac{1}{R_H \cdot C_H} \, s + \frac{1}{L_H \cdot C_H}} \tag{4}$$

Equating the s terms and the real terms of equations 3 and 4 provide the half-circuit values for C_H and L_H, respectively. These values are for the case where $\omega_0 = 1$ radian per second and should be frequency scaled by dividing through by $\omega_0 = 2\pi f_C$.

$$C_H = \frac{1}{\sqrt{2} \cdot R_H} = \frac{1}{2 \cdot \pi \cdot f_C \cdot \sqrt{2} \cdot R_H} \tag{5}$$

$$L_H = \frac{1}{C_H} = \sqrt{2} \cdot R_H = \frac{\sqrt{2} \cdot R_H}{2 \cdot \pi \cdot f_C} \tag{6}$$

Two half-circuit models are then combined to yield the actual BTL circuit as shown in Figure 4. The capacitors and resistors are then combined to provide the final BTL equations.
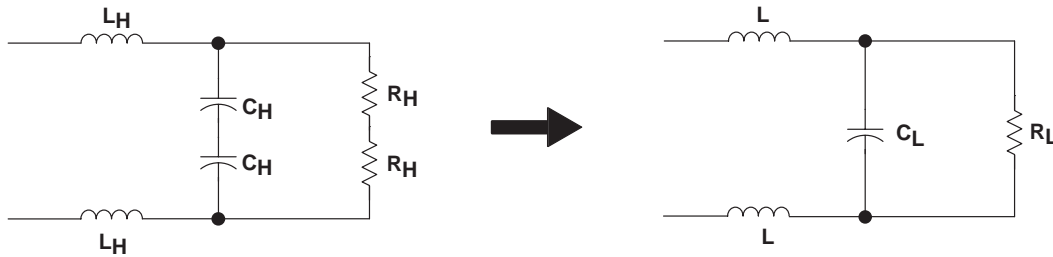
Figure 4. Combination of Two Half-Circuit Models

$$R_L = 2 \cdot R_H \tag{7}$$

$$C_L = \frac{1}{2\sqrt{2} \cdot \pi \cdot R_L \cdot f_C} \tag{8}$$

$$L = L_H = \frac{\sqrt{2} \cdot R_L}{2 \cdot \omega_0} = \frac{\sqrt{2} \cdot R_L}{4 \cdot \pi \cdot f_C} \tag{9}$$

The inductor values actually remain the same for the half- and full-bridge circuit since there are two inductors in the BTL circuit. The –3-dB cutoff frequency for the LC filter, based on the BTL values, is

$$f_C = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot LC_L}} \tag{10}$$

where the $\sqrt{2}$ in the denominator is the result of transposing the values for L and C from the half-circuit model to the full BTL circuit.

Table 1 shows values for L and C_L for a given f_C and R_L.

Table 1. Second-Order Butterworth LC_L Values

DC LOAD RESISTANCE (R_L – Ω)	CUTOFF FREQUENCY (f_C – kHz)	INDUCTOR VALUE (L – μH)	CAPACITOR VALUE (C_L – μF)
4	20	22.5	1.41
4	25	18	1.13
4	30	15	0.94
4	35	12.9	0.80
8	20	45	0.70
8	25	36	0.56
8	30	30	0.47
8	35	26	0.40

The capacitors labeled C in Figure 2 serve as high frequency bypass capacitors, and are empirically chosen to be approximately 10% of $2 \cdot C_L$. Their small value has a negligible impact on the filter cutoff frequency.

The choice of filter components and f_C may dictate the use of a series RC Zobel network placed in parallel with the load.[1] This depends on the Q of the circuit, which changes when a speaker, which is highly reactive, is connected as the load.

2.2.2 Design Example

The class-D audio system will have a passband of 20 Hz to 20 kHz and a switching frequency (f_S) of 250 kHz. The pass-band attenuation of f_S should be 40 dB, and the corner frequency of the LPF will be set to avoid attenuating audio signals by more than 1 dB across the audio spectrum. The speaker dc resistance is 4 Ω. A second-order LC filter is to be used. What inductor and capacitor values are required?

The inductance and capacitance are calculated using the BTL equations:

$$C_L = \frac{1}{2 \cdot \pi \cdot \sqrt{2} \cdot R_L \cdot f_C} = \frac{1}{2 \cdot \pi \cdot \sqrt{2} \cdot 4\Omega \cdot 25 \text{ kHz}} = 1.1\mu F \tag{11}$$

$$L = \frac{\sqrt{2} \cdot R_L}{4 \cdot \pi \cdot f_C} = \frac{\sqrt{2} \cdot 4\Omega}{4 \cdot \pi \cdot 25 \text{ kHz}} = 18 \ \mu H \tag{12}$$

These values are checked by substituting into equation 10 and found to be correct. Reviewing available component values shows options for L of 15 μH and 22 μH, and the closest value for C_L is 1 μF. The values for C_L = 1 μF and L = 15 μH push the filter cutoff frequency out to 29 kHz.

The filter is now complete, except for the high frequency bypass capacitors labeled C in Figure 2. These capacitors should be approximately 10% of $2 \cdot C_L$, or 0.2 μF. The nearest standard value of 0.22 μF is selected.
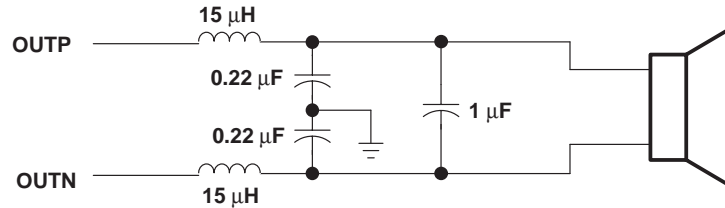
Figure 5. Complete BTL Output Filter

2.2.3 Component Selection

The output inductors are the key elements in the performance of the class-D audio power amplifier system. The most important specifications for the inductor are the dc resistance and the dc and peak current ratings. The dc resistance directly impacts the efficiency by adding to the total load resistance seen by the power supply. An approximation of the efficiency is

$$\eta = \frac{POUT}{PIN} = \frac{I^2 \cdot R_L}{I^2 \left[2 \left(R_{DSON} + R_{IND}\right) + R_L\right]} \tag{13}$$

where R_L is the dc resistance of the speaker, R_{DSON} is the on resistance of the DMOS power transistors, and R_{IND} is the dc resistance of the inductors.

The inductor current ratings must be high enough to avoid magnetic saturation, which will cause an increase in audio signal distortion or, if completely saturated, will cause the inductor to appear as a short rather than an open circuit to the PWM output. This could potentially damage the device or speakers from the resulting high current surge that may occur during turn on, or the increased quiescent current during normal operation. It would seem best, then, to choose an inductor that has a much higher current rating. The tradeoff is that the size and cost increase as the current capability increases. Shielded inductors will also help reduce distortion and EMI, minimizing crosstalk in the process.

The filter capacitors should be ceramic capacitors with X7R characteristics for stability over voltage and temperature, and can be found in common surface-mount packages as small as 0805. The values of capacitance calculated in the example above are readily available in ceramic chip and metal film capacitor product lines. Measurements have shown little difference between the performance of these two types of capacitors, though some audiophiles will strongly recommend the metal film. The capacitors should be rated to handle the sum of the dc and ac voltages, which will be

$$V_{CAP} = \left(\frac{V_{SUPPLY}}{2}\right) + \left(0.707 \cdot \sqrt{P_{MAX} \cdot R_L}\right) \tag{14}$$

where V_{SUPPLY} is the power supply input voltage, P_{MAX} is the maximum rms power output for the amplifier, and R_L is the dc resistance of the speaker. This is the minimum supply voltage needed, and allowances must be made for temperature, applied voltage, and transient voltage spikes. As a rule of thumb, the voltage rating should be twice what is calculated.

2.3 Charge Pump Circuit

The charge pump circuit consists of one or more external charge pump capacitors, an external charge storage capacitor, and an internal circuit that controls the flow of charge in the circuit. Figure 6 shows the internal and external components and functions that make up a tripler charge pump circuit where C_{CP1} and C_{CP2} are the charge pump capacitors and C_{VCP} is the charge storage capacitor.
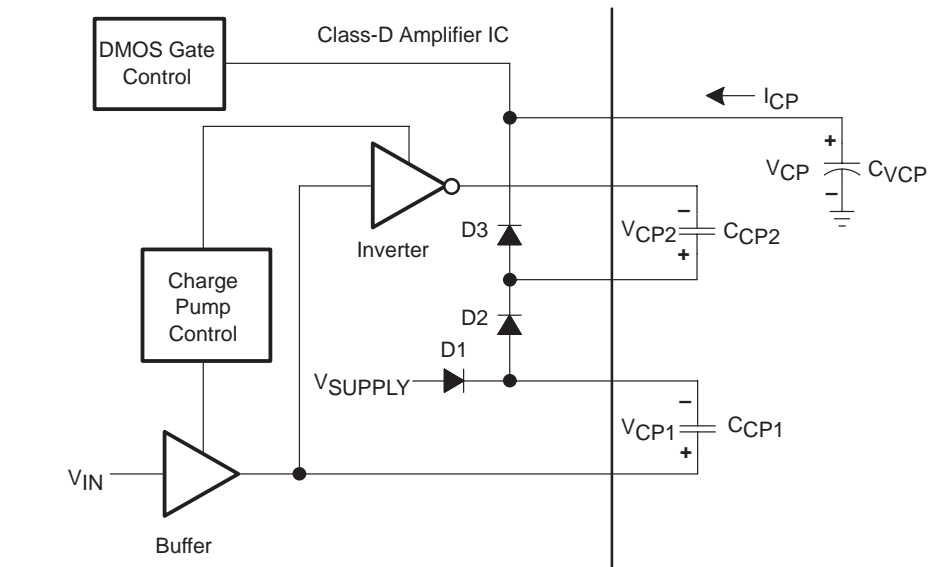

Figure 6. Tripler Charge Pump Circuit

V_{IN} is a switching waveform that transitions between V_{SUPPLY} and 0 V. When V_{IN} is low, the output of the buffer is low, D1 is on, and C_{CP1} charges to V_{SUPPLY}. The inverter then provides a high output voltage to C_{CP2}, D2 remains off, preventing any charge transfer from C_{CP1} to C_{CP2}, and D3 turns on. Charge is then shared between C_{CP2} and C_{VCP}. When V_{IN} goes high the buffer output goes high, and the voltage across C_{CP1} becomes $(2 \cdot V_{IN})$, turning D1 off. The inverter output simultaneously provides a low output to C_{CP2}, turning D2 on and D3 off. Charge from C_{CP1} is then shared with C_{CP2}. This process continues until the charge builds up and V_{CP} is in the operational range of $(V_{SUPPLY} + 6V)$ to $(3 \cdot V_{SUPPLY})$ for a charge tripler, and $(V_{SUPPLY} + 6V)$ to $(2 \cdot V_{SUPPLY})$ for a charge doubler. The charge from C_{VCP} is then used to drive the DMOS output transistor gates.

The value for V_{CP} must be large enough to supply the charge required by the DMOS gate capacitance, yet small enough to fully charge within one-half of the class-D switching period. If these conditions are not met, C_{VCP} fails to fully charge during each switching cycle the $R_{DS(ON)}$ can increase substantially and degrade the operation of the DMOS output transistors.

The proper capacitance is recommended in the device data sheets and in evaluation module user guides. The values required for these capacitors are relatively small and are readily available in surface-mount ceramic chips. The capacitors must be relatively stable over the expected operating temperature. Good quality X7R, ±10% ceramic capacitors should be used with voltage ratings greater than the maximum voltage of the charge pump, V_{CP}, stated in the device data sheets. Power dissipation is not a factor in this circuit as the currents are low and the frequency of operation is high.

2.4   Switching Circuit

The switching circuit consists of a ramp generator and compensation capacitors for each channel. These circuits all require external capacitors in order to function. Selection of these capacitors is important for providing a balanced triangular waveform and accurate regulation of the duty cycle for the output transistors. The switching circuit is identical for each channel of the class-D amplifier. Figure 7 shows the switching circuit for the right channel.
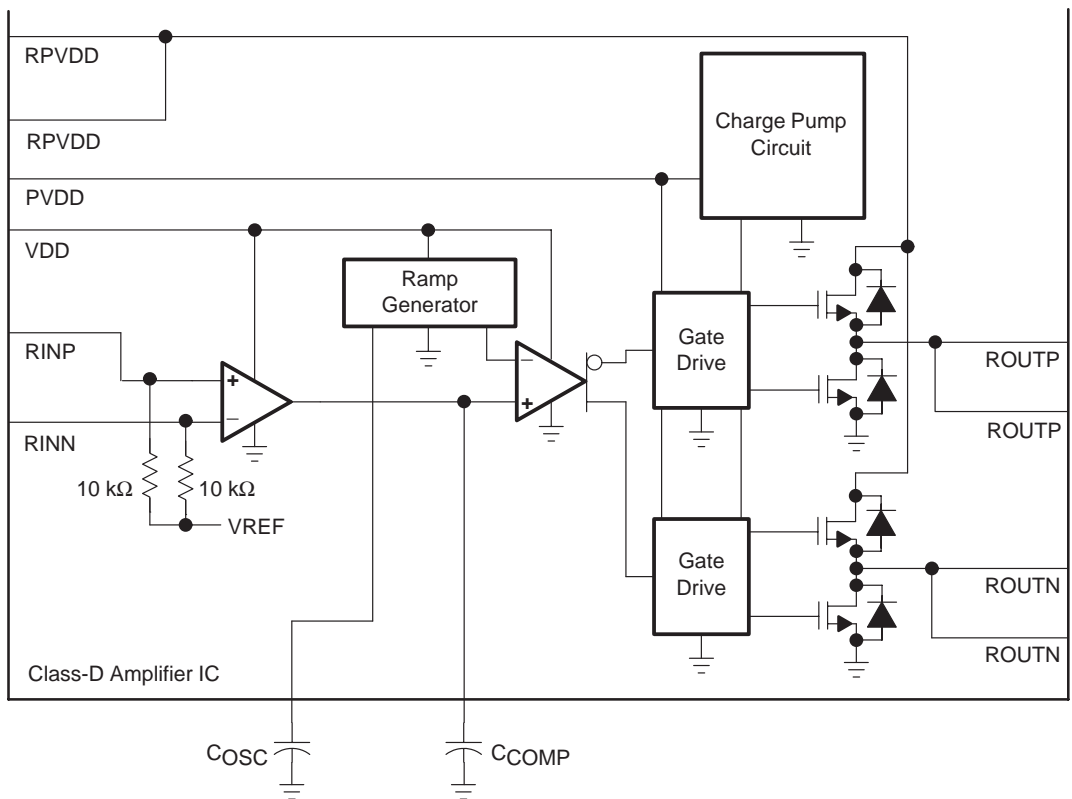

Figure 7. Switching Circuit for the Right Channel

The ramp generator is the heart of the class-D amplifier — it sets the operational frequency for the system from 100 kHz to 500 kHz. Oscillator capacitor C_{OSC} charges and discharges at a constant rate with an applied constant current to form a triangular waveform that is applied to one input of the comparator. The capacitance is directly proportional to the period — doubling the capacitance doubles the length of the period, decreasing the switching frequency (f_S). The data sheets and EVM user guides provide the value of capacitance required to generate a nominal f_S of 250 kHz. Knowing the value of this capacitance (C_{250}), f_S, and the desired switching frequency, the new capacitance, C, can be easily calculated for any desired frequency of oscillation, f, from the ratio of two capacitors as shown in equation 15.

$$C_{OSC} = C_{250} \cdot \left(\frac{f_S}{f} \right) \tag{15}$$

The compensation capacitors, C_{COMP} are used to stabilize the comparator inputs and should be identical to C_{OSC}. Ceramic capacitors with C0G temperature characteristics are the common type available in such a small capacitance. These capacitors do not exhibit a change in value with changing ac or dc voltages, and are extremely stable over large temperature ranges. A standard 50-V C0G-type capacitor with a maximum of ±5% tolerance is recommended, with much tighter tolerances available if desired.

3   Headphone Circuit

Some of the class-D amplifier ICs feature class-AB headphone (HP) amplifier circuits capable of driving 50 mW of power into a 32-Ω load from a 5-V supply. TTL-compatible interface logic (a mode pin) is provided to select between class-D or class-AB modes of operation. Each HP channel consists of an internal operational amplifier and pins for connecting external components that control the gain and filtering for the headphones.

Class-D EVMs are available that integrate the HP amplifier functions. A typical channel of the HP circuit for such an EVM is shown in Figure 8. External pins on the EVMs allow easy connections to the inputs and outputs, and a miniature headphone jack has been provided on the EVM board for easy testing of the HP amplifier. The HP jack includes the control pins necessary to control the IC mode. An onchip regulator provides the 5 V required for operation of the HP amplifier circuit. The power decoupling capacitor, C, is discussed in the *Device Power Supply Decoupling* section of this report. Capacitor C_{V2P5} stabilizes the HP circuit, and should be the size recommended in the data sheets and the EVM user guides.
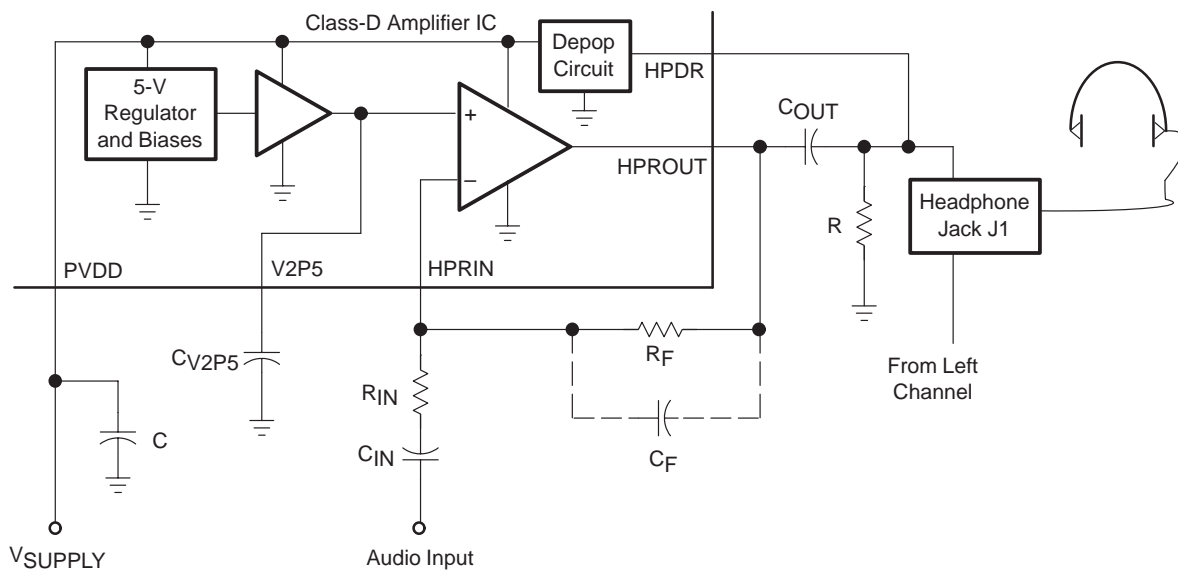
Figure 8. Headphone Amplifier Circuit, Right Channel

Each amplifier is configured as an inverting operational amplifier with externally controlled gain. The transfer function for this circuit, ignoring C_{OUT}, R, and any load resistance, R_L, is shown in equation 16 where $\omega_1 = (C_F \cdot R_F)^{-1}$ and $\omega_2 = (C_{IN} \cdot R_{IN})^{-1}$.

$$H(j\omega) = \frac{V_O}{V_{IN}} = \frac{\left(-\dfrac{R_F}{R_{IN}}\right)}{\left(1 + \dfrac{\omega_1}{j\omega}\right)\left(1 + \dfrac{j\omega}{\omega_2}\right)} \tag{16}$$

Input capacitor C_{IN} serves to ac-couple the input. The series combination of R_{IN} and C_{IN} in this circuit creates a LPF function in the denominator, which then acts as a HPF to set the low frequency corner shown in equation 17, where $R = R_{IN}$ and $C = C_{IN}$. f_{LO} can be easily adjusted by changing C_{IN} or R_{IN}.

$$f_{LO} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{17}$$

Capacitor C_F is recommended for stability purposes when the gain is greater than or equal to –10 V/V. The parallel combination of R_F and C_F then creates a HPF function which, when in the denominator, acts as a LPF to set the high frequency corner (f_{HI}) of the circuit. equation 17 may be used to calculate f_{HI}, with $R = R_F$ and $C = C_F$. This corner frequency should be about 300 kHz, well above the audio band.

Capacitor C_{OUT} is required for all single-ended audio circuits to ac-couple the output, preventing dc current from flowing into the HP. C_{OUT} forms another LPF in conjunction with the dc resistance (R_L)of the headphones. Resistor R may be included if the IC mode control interface is implemented with the HP jack, and is much larger than R_L and can be ignored in this analysis. The class-D EVMs with HP amplifiers use such a circuit. equation 17 is again used to calculate the low frequency corner for this filter. It should be noted that the corner frequencies of the input and output filters will overlap to some degree.

The HP circuit includes some internal depop circuitry that is used to minimize the pop in the speakers when the HP is activated and deactivated. The largest capacitor that is recommended for use with this circuit is 33 μF. Higher values may be used, but will decrease the effectiveness of the depop circuit.

Ceramic capacitors are available for the small values of capacitance used for the input and feedback path. The voltage rating of the input capacitor will depend upon the gain of the circuit, which should be greater than the passband gain (A_V) in equation 18.

$$A_V = \left| \frac{R_F}{R_{IN}} \right| \tag{18}$$

This is then used to calculate the maximum input voltage in equation 19.

$$V_{IN} = \frac{5V}{A_V} \tag{19}$$

The voltage rating of the feedback capacitor should be a minimum of 5 V, and is readily available in a $\pm$5% C0G package for such a low capacitance. The input capacitors are larger and available in a $\pm$10%, X7R package, depending upon the value.

4   Control and Indicator Circuits

The Texas Instruments class-D audio power amplifiers have three main control input pins (shutdown, mute, and mode) for external control of chip functions. Each of these inputs is TTL compatible to allow easy interface with logic. The shutdown and mute controls are provided with each class-D device, while the mute control is only applicable to devices that incorporate a class-AB headphone amplifier.

Two indicator pins (fault0 and fault1) are also provided to allow monitoring of chip status. They provide feedback when an under-voltage, over-current, or thermal fault exists. These pins are provided on each of the devices.

4.1   Shutdown

The shutdown control pin allows the device to be placed into a power-saving sleep mode to minimize current consumption. This pin is TTL active low — a voltage of less than 0.8 V at this pin will shut down the entire device. The device will become active when the voltage at the pin rises above 2 V. When in shutdown, the IC draws a maximum quiescent current that is less than 1 μA.

In typical applications, as often found in notebook computers, portable audio products, and such, the internal speakers mute when headphones are plugged into the headphone jack, or internal speakers mute when external speakers are connected. In applications using separate speaker and headphone amplifiers, the one not being used can be shut down to conserve power.

4.2   Mute

The mute control pin turns on the low-side output transistors, shorting the load to ground and muting the outputs of the device. This pin is TTL active low — a voltage of less than 0.8 V will mute the device outputs. The outputs will turn on when the voltage at the mute pin rises above 2 V. When muted, the class-D device draws only a few mA of quiescent current.

4.3   Mode

The mode control pin selects either the class-D or the headphone amplifier as the active amplifier, placing the inactive amplifier in a power-saving sleep mode. This pin is TTL compatible, with a voltage less than 0.8 V activating the class-D amplifier, and a voltage greater than 2 V activating the headphone amplifier.

This function can easily be controlled with a headphone jack that contains an internal switch to change the state of the control line, and has been successfully implemented on the EVMs for the class-D amplifiers that integrate headphone circuits. Figure 9 shows an example of this type of circuit.
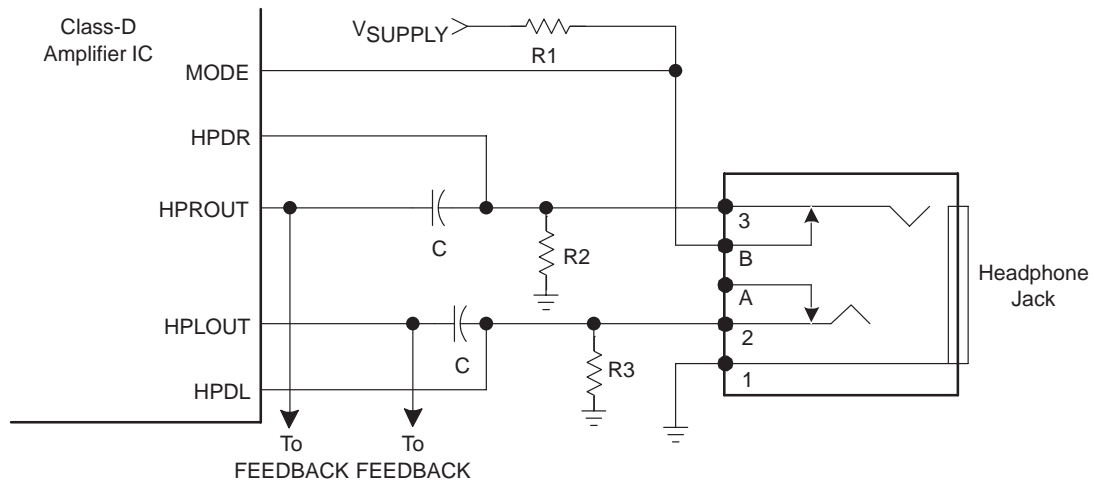

Figure 9. Mode Control Circuit Featuring Headphone Jack Control

Resistors R1 and R2 form a divider network when a headphone plug is not inserted into the headphone jack. The ratio of these resistors should be such that the mode pin is held below 0.8 V to activate the class-D amplifier. When a headphone plug is inserted into the jack, contact B is disconnected from pin 3 of the jack and no current flows through R1, causing the mode pin to float to V_{SUPPLY}. This deactivates the class-D amplifier and activates the headphone amplifier. Removal of the headphone plug from the jack then connects contact B to pin 3 and pulls the MODE pin low, causing the device to revert to class-D operation. Resistor R3 is included in the remaining channel to balance the outputs of the two channels when the headphone amplifier is active.

4.4 Fault Indicators

Two fault indicator pins on the class-D amplifier IC provide feedback when a fault condition exists. Signals on these pins indicate the status of the class-D amplifier: operational, over-current, thermal fault, and under-voltage lockout. The only status reported for the class-AB headphone amplifier is for a thermal fault, which is indicated by the same error code as for the class-D amplifier. The device data sheets list the error codes for each of these conditions.

The TTL-compatible fault pins are connected to open drain outputs and require a pullup resistor to limit the current flow into the pins to a maximum of 1 mA. Once a fault is triggered, the appropriate fault pins remain active until the fault is cleared by cycling the shutdown pin, mute pin, or the power supply to the device.

5 Device Power Supply Decoupling

Adequate delivery of power and proper grounding reduces distortion and ensures correct operation of the class-D device. Power supply filtering and appropriate ground connections are discussed below.

Power supply filtering has two objectives: decouple the power supply from the class-D amplifier and provide a path for high frequency noise to bypass the device. There are three main power inputs for the device: class-D analog input and controls (VDD), charge pump and headphone (PVDD), and the output (RPVDD and LPVDD). Figure 10 shows the power bus and recommended filtering for a class-D audio power amplifier.
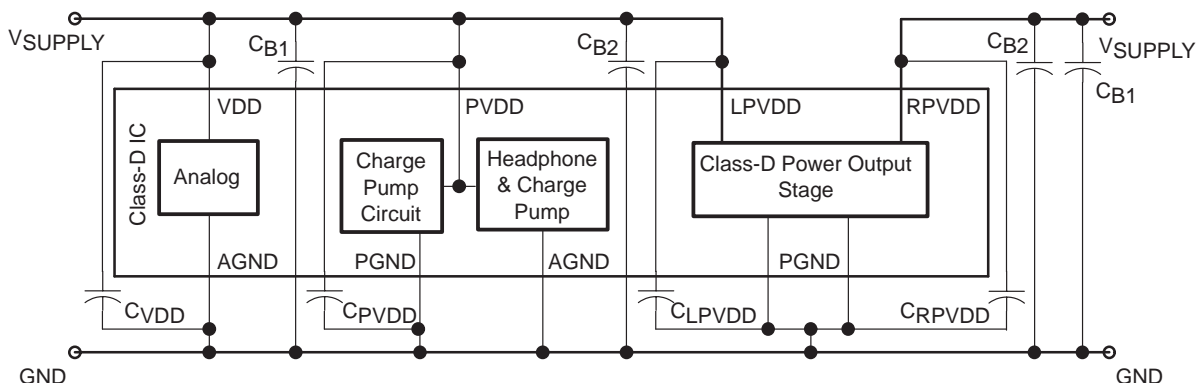

Figure 10. Class-D Power Bus, 48-Pin TSSOP Package

All of the capacitors connected to the power bus (V_{SUPPLY}) are working to decouple the circuit from the power supply. The large bulk capacitors (C_{B1} and C_{B2}) are provided for each channel to supply the majority of the switching current required by the amplifier. Smaller capacitors (C_{VDD}, C_{PVDD}, C_{LPVDD}, and C_{RPVDD}) are placed adjacent to the various power pins to supply the initial charge of the switching current. The only power pins located on the right side of the chip (RPVDD) are for the high power output section of the right channel. The remaining power pins (VDD, PVDD and LPVDD) are located on the left side of the chip and will be the focus of the discussion. The right channel capacitors will then be identical to those of the left channel.

5.1 Bulk Capacitors

Real-world capacitors are modeled using parameters such as equivalent series resistance (ESR), equivalent series inductance (ESL), capacitive reactance (X_C) and inductive reactance (X_L). The equivalent impedance of a capacitor over frequency is simply modeled by

$$Z = \sqrt{ESR^2 + (X_c - X_L)^2}$$

(20)

X_L is small for frequencies below 1 MHz and can be neglected since the switching frequency range of the TPA005D14 is 100 kHz to 500 kHz. The capacitive reactance is maximum and dominates at dc. It decreases as the frequency increases until resonance is reached ($X_C = X_L$), at which point Z = ESR. The ESR of a capacitor is considered to be constant over the 100 kHz to 500 kHz switching frequency range of the class-D amplifier, and is usually provided by the manufacturer.

The values for the bulk capacitors C_{B1} and C_{B2} are the primary concern, and are calculated using the circuit shown in Figure 11. It is assumed that L_{IN} is large (steady current flows from the power supply) and has a negligible ripple, the capacitor current for C is negligible, and the switching frequency and dc load resistance is known.
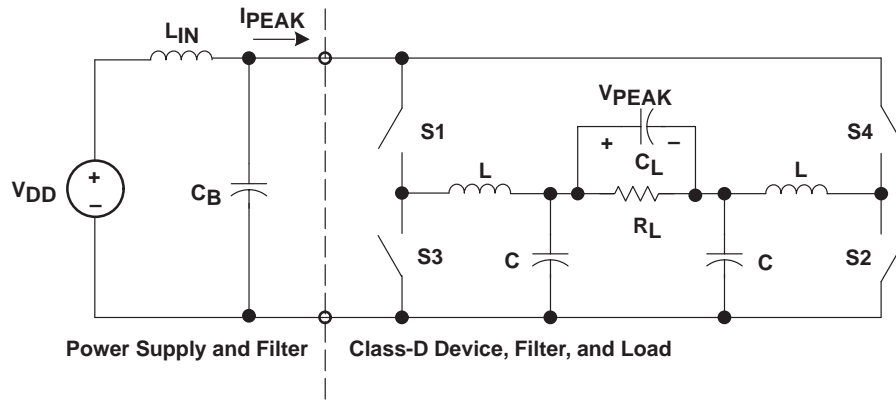

Figure 11. Power Supply Bulk Decoupling Capacitor Circuit

The peak power for a given load is then used to calculate the peak voltage, which is then used to calculate the peak current.

$$V_{PEAK} = \sqrt{P_{PEAK} \cdot R_L} \tag{21}$$

$$I_{PEAK} = \frac{V_{PEAK}}{R_L} \tag{22}$$

This current flows from C_B through S1, the load, and S2 to ground. The minimum capacitance required to supply this peak switching current is

$$C = \frac{I_{PEAK} \cdot T_D \cdot D_{MAX}}{V_{RIPPLE}} \tag{23}$$

where $T_D = 1/f_{switch}$ is the period, D_{Max} is the maximum duty cycle, and V_{Ripple} is the desired ripple voltage, or droop, that will appear at the output of the amplifier. This is the capacitance required to limit the ripple voltage based on the capacitance alone. In most every case, the ripple voltage caused by the ESR will dominate. The maximum ESR required to achieve the same V_{Ripple} for the same I_{Peak} from equation 22 is calculated in equation 24 below.

$$ESR = \frac{V_{RIPPLE}}{I_{PEAK}} \tag{24}$$

The total ripple voltage contributed by the bulk capacitor C_B is the sum of equations 23 and 24. The requirements of the application will determine the acceptable tradeoffs in the selection of components that meet these criteria. It should be noted that the total ripple voltage seen at the output of the class-D amplifier will be approximately equal to that calculated in equation 25.

$$V_{RIPPLE}^{MAX} = I_{PEAK} \left[\left(\frac{T_D \cdot D_{MAX}}{C} \right) + ESR + R_{DS(ON)} \right]$$ (25)

There are various ways to implement the bulk capacitance that is selected: one large capacitor that meets the requirements of both equations (23) and (24) can be used; two or more capacitors can be paralleled to reduce the ESR and the size of the capacitors; or two different types of capacitors can be used to supply the current and meet the ESR specifications. Keep in mind that the ESR of the actual capacitor used should be 30% – 50% lower than the calculated value to allow for increases due to temperature, ESL, and aging.

Electrolytic capacitors, aluminum or tantalum, are the best choice right now for large capacitance requirements, though ceramic capacitors of up to 100 µF are being produced in low voltage packages. The electrolytic capacitors are normally useful for applications below 1 MHz. This is due to their low resonant frequency and is the reason for using smaller, ceramic capacitors in parallel with the electrolytic. Electrolytic capacitors, in particular the tantalum type, are subject to damage by stress from exceeding the voltage rating. They must be chosen such that they will retain the minimum required capacitance and maximum ESR over the entire temperature range and for the voltage range to avoid damage and early failure of the components. The voltage rating should be greater than the sum of the supply voltage and the total maximum ripple voltage of equation 24.

5.2 Small Decoupling Capacitors

The large capacitance of C_{B1} and C_{B2} means a slower response time due to the large time constant formed with the resistance of the circuit, and is why the smaller capacitors C_{VDD}, C_{PVDD}, C_{LPVDD} and C_{RPVDD} are used. These capacitors provide a smaller time constant for a much quicker discharge time, and supply the initial transient charge required for the high frequency switching pulses of the class-D amplifier. Their low value pushes the resonant frequency of the capacitor out — they appear capacitive at much higher frequencies due to the smaller X_L of equation 20. This serves to bypass unwanted high frequency signals.

The current for the VDD pin is very low and can have the transient requirements satisfied by a 0.1 µF or 1 µF capacitor. The PVDD pin will draw less than 100 mA of current and should have a 1-µF decoupling capacitor. These must have a voltage rating that is greater than the sum of the supply voltage and the maximum ripple voltage of equation 25.

The values required for these capacitors are small and readily available in surface-mount ceramic chips. The capacitors should be relatively stable over the expected operating temperature. Good quality X7R, ±10% ceramic capacitors are available for the capacitance required, though ±20% or +80/–20% Y5V capacitors may be used, depending upon the application. Power dissipation is a factor in this circuit as the currents can be quite high.

6   PCB Layout

Good layout practices and well thought out design provide excellent performance for the TI class-D audio power amplifiers. There are three main areas of concern in the layout: the ground plane, power plane, the inputs and the outputs. Each is discussed briefly below. See the TI website for more information on class-D layouts.

6.1   Ground Plane

Experimentation with several types of ground planes has shown that, with some careful planning and good layout practices, a solid ground plane works as well as other types of grounding schemes. This is due in part to the relatively low frequencies of operation for the system, and to the careful layout of the components and traces. The solid ground plane also serves to assist the PowerPAD[2] in the dissipation of heat, keeping the class-D amplifier relatively cool and negating the need for an external heat sink. Connection to the PowerPAD is discussed later in this section. Finally, the ground plane can act as a shield to help isolate the power pins from the output, reducing the impact of EMI on the traces and pins.

It is important that any components connecting an IC pin to the ground plane be connected to the nearest ground for that particular pin. Table 2 lists the ground pins for the various sub-circuits that are part of the TPA005D14 class-D IC to assist in determining where a component should be grounded. Care should be taken to prevent the ground return path of any high current components (such as the output filter capacitors) from directly passing through other ground connections of the IC, particularly the input.

Table 2. Audio Power Amplifier Subcircuit Ground Pins

GROUND PIN No.	APPLICABLE CIRCUITS	TPA005D14 RELATED PINS[†]
47	Controls (shutdown, mute, mode)	1, 2, 3
	Class-D outputs	4, 5, 44, 45
	Ramp generator	6, 43, 48
	Grounds	7, 46
	Input power (VDD)	8
	Fault indicators	41, 42
12, 13, 36, 37	Output power (LPVDD, RPVDD)	9, 16, 33, 40
	Class-D outputs	10, 11, 14, 15, 34, 35, 38, 39
20	Headphone	17, 18, 19, 23, 26, 29, 30, 31, 32
27	Charge pump	21, 22, 23, 24, 25, 26, 28

[†] Pin numbers may vary in other class-D devices.

6.2 Power Plane

There are three main power sections on the chip: the input circuit power pins (VDD), the output stage power pins (LPVDD and RPVDD), and the power for the headphone and charge pump circuits (PVDD), as shown in Figure 9. When the device is operating (i.e. audio is being applied to the amplifier), the VDD pin draws only a few mA of current and the PVDD pins draw several tens of mA. This is in sharp contrast to the amps of current drawn by the LPVDD and RPVDD pins.

The power traces are kept short and the decoupling capacitors placed as close to the power pins as possible. This is particularly true for the small decoupling capacitors that are to be placed adjacent to each IC power pin. Terminate the capacitor ground close to the ground for the particular power section as possible while paying attention to ground return current paths. This minimizes ground loops and provides very short ground return paths and high frequency loops.

The VDD pin supplies power for sensitive analog circuitry and is the most sensitive pin of the device. It must, therefore, be kept as noise free as possible. The demand for peak current is small and mostly satisfied by the charge of the small decoupling capacitor. The PVDD pin(s) are not as sensitive to noise as the VDD pin. They supply the current for the headphone regulator and control circuits when the device is in class-AB mode (when applicable), and the charge pump circuit when in class-D mode. The power traces for these power inputs should be connected to the main power bus at a point near the large decoupling capacitor(s). The small inductance of the traces and the charge supplied by the large decoupling capacitor greatly reduces the ripple current of the main power bus seen by these pins. Terminate the capacitor ground side close to the ground for the particular power section while paying attention to ground return current paths. Again, this minimizes ground loops and provides very short ground return paths and high frequency loops.

The main power bus should terminate into the LPVDD and RPVDD pins, with the small decoupling capacitors for each channel placed adjacent to each pair of pins. When more than one bulk capacitor is used, place the smaller of the two between the power pins and the large bulk capacitor. These traces should be wide enough to handle the maximum peak current per channel over the operating temperature range, and symmetric to facilitate even power distribution. Place them directly over the ground plane to reduce EMI and minimize the ground return path.

6.3 Inputs and Outputs

The pinout of the class-D amplifiers facilitates the separation of the inputs and outputs, enabling isolation of ground return paths and high frequency loops. The class-D and headphone amplifier input traces should be kept as short as possible between the ac coupling capacitors and the amplifier IC input pins to reduce noise pickup. Keep the inputs separated from the outputs, particularly from the inductors if unshielded units are used, to minimize magnetic coupling. The headphone traces may be in close proximity with the class-D output since the two amplifiers are not active at the same time.

The control (shutdown, mute, and mode) input pins have almost no current flow through them, and inductance and resistance of the traces is of a minimal concern. The indicator output pins (fault0 and fault1) have less the 1 mA of current flow, and should be sized accordingly. There are no special considerations for the layout of these traces — standard layout practices will apply.

It is critical to minimize the trace lengths between the device class D output pins and the LC filter components, particularly those that contain the full square wave. The traces to the inductors should be kept short, yet separated from the input circuit as much as possible. Routing the pre-inductor output traces of a particular channel (i.e., ROUTP and ROUTN) on adjacent layers so that they overlap will cause the magnetic fields to subtract from each other, reducing the EMI. All high-current output traces should be wide enough to allow the maximum peak current to flow over the entire operating temperature range of the system. Failure to do so will create excessive voltage drops, a decrease in efficiency, and an increase in distortion.

6.4 General PowerPAD Considerations

The class-D IC is mounted in a special package that incorporates a thermal pad designed to transfer heat from the silicon die of the IC directly to the PCB. The PowerPAD™ package is constructed using a downset leadframe. The die is mounted on the leadframe with the chip ground tied to the pad through a low impedance. The bottom surface of the leadframe is exposed and serves as a metal thermal pad on the underside of the IC package. This metal is then soldered directly to the PCB, providing direct contact between the die and the PCB etch, which, in turn, provides an exceptional thermal transmission path. Excellent thermal performance can then be achieved by providing this thermal path on the PCB.

The following steps illustrate the recommended approach to properly heatsink a TI class-D audio power amplifier 48-pin DCA package that integrates the PowerPAD with a circuit board.

1. Prepare the PCB for proper connection to the class-D IC with a top layer etch pattern as shown in Figure 12. Etch should be provided for both the IC leads and the PowerPAD.
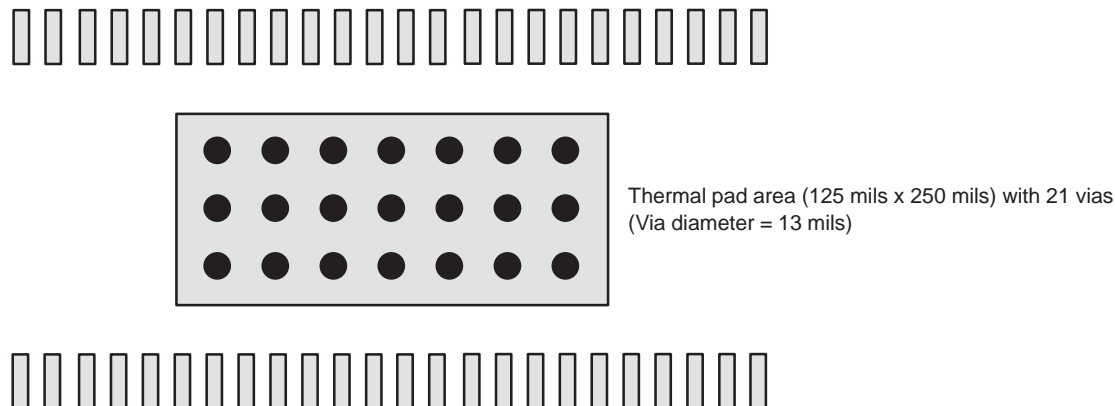

Thermal pad area (125 mils x 250 mils) with 21 vias (Via diameter = 13 mils)

Figure 12. PowerPAD PCB Etch and Via Pattern

2. Place 21 vias evenly spaced in three rows (seven per row) in the area for the PowerPAD. These vias should be 13 mils in diameter to minimize solder wicking through the holes during reflow soldering, ensuring a good connection between the IC thermal pad and the PCB etch.

3. Additional vias may be placed anywhere along the thermal plane outside of the PowerPAD area to assist with heat dissipation. These vias are not restricted to the 13 mils of step 2 since they are not used to connect the IC to the PCB.

4. Connect all of these vias to the PCB ground plane. The ground plane now becomes the heatsink for the amplifier IC.

5. Do not use a web or spoke connection when connecting these vias to the ground plane. Web connections have a high thermal resistance that is used to slow heat transfer to the ground plane, making soldering of these vias easier. This would impair the flow of heat between the PowerPAD and the circuit board ground plane and is not recommended.

6. The solder mask on the top layer should then leave the etch pads for the IC pins and PowerPAD exposed. The bottom layer solder mask should, however, cover the entire thermal pad as well as the via edges, leaving tiny holes in the very center of each via. This prevents the solder connecting the IC thermal pad to the PCB from being wicked away during reflow.

7. Apply solder paste to the exposed etch pads for the IC pins and PowerPAD.

8. The class-D IC is then soldered in position during the reflow process. Actual thermal performance achieved with the package will depend upon the application. The Texas Instruments Technical Brief, *PowerPAD Thermally Enhance Package*, Literature Number SLMA002, contains more information on the PowerPAD package and its thermal characteristics.

7 References

[1] The Texas Instruments application report, *Reducing and Eliminating the Class-D Output Filter*, literature number SLOA023.

[2] The Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package*, literature number SLMA002, contains more information on the PowerPAD package and its thermal characteristics.